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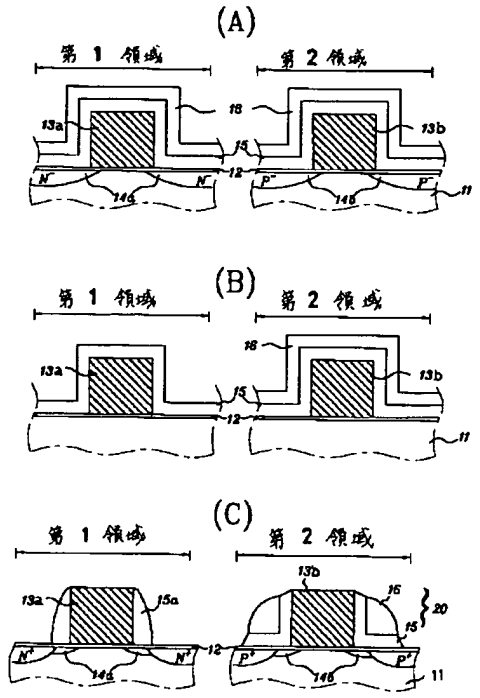
(54)【発明の名称】　半導体素子の製造方法

(57)【要約】

【課題】　ショートチャネル特性を改善し、素子の駆動電流を増加する。

【解決手段】　第1領域及び第2領域に夫々形成されるポリシリコンゲート１３ａ，１３ｂ上に、湿式食刻に選択比の優れた酸化膜及び窒化膜からなる第1絶縁膜１５及び第2絶縁膜１６を形成した後、第2絶縁膜１６上に感光膜をコーティングする。そして、側壁スペース１５ａ，２０の形成箇所の感光膜を除去してから異方性食刻を施すことで、選択的に側壁スペース１５ａ，２０が形成される。この際、第2領域において第1絶縁膜１５及び第2絶縁膜１６から側壁スペース２０を形成するようにして、側壁スペース２０の厚さを側壁スペース１５ａの厚さより厚くし、ショートチャネル特性を改善する。



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2

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VLSI 1991.p.

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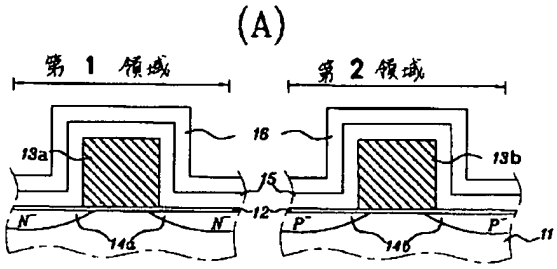
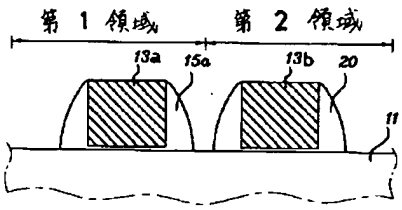
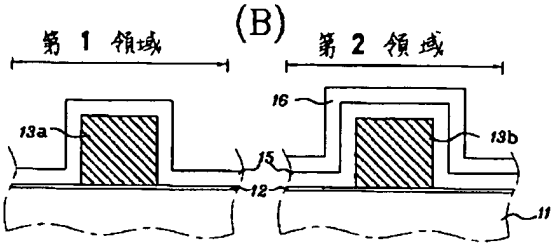
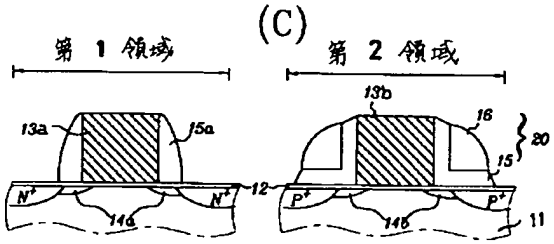
Lightly Doped

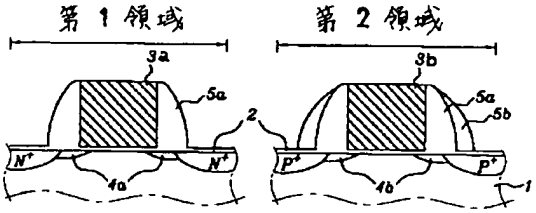
Drain

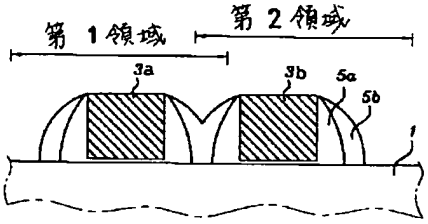












(51)Int.Cl.

21/8242

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SEMICONDUCTOR DEVICE MANUFACTURING METHOD

CLAIM(S)

1) A semiconductor device manufacturing method being comprised of:

a step of forming a gate insulating film 12 on a semiconductor substrate 11 having a first region and a second region;

a step of forming a first gate electrode 13a and a second gate electrode 13b on the first region and the second region on the semiconductor substrate 11, respectively;

a step of forming a first conduction-type low concentration impurity region near the base of said first gate electrode 13a in the first region on the semiconductor substrate;

a step of forming a second conduction-type low concentration impurity region near the edge of the base of the second gate electrode 13b in the second region on the semiconductor substrate;

a step of forming a first insulating film 15 on the semiconductor substrate 11 on which are formed the first and second gate electrodes, 13a, 13b;

a step of forming a second insulating film 16 on the first insulating film 15;

a step of removing the second insulating film 16 in the first region;

a step of forming a first sidewall space 15a on the side surface of the first gate electrode 13a by anisotropic-etching the first insulating film 15 in the first region;

a step of forming a first conduction-type high concentration impurity region 14a near the edge of the base of the first gate electrode 13a in the first region where the first sidewall space 15a is formed;

a step of forming a second sidewall space 20 made of first insulating film 15 and second insulating film 16 on the side surface of second gate electrode 13b by anisotropic-etching the first insulating film 15 and second insulating film 16;

a step of forming a second conduction-type high concentration impurity region 14b near the edge of the base of the second gate electrode 13b on

which the second sidewall space 20 is formed in the second region on the semiconductor substrate.

2) A semiconductor device manufacturing method, as cited in Claim 1, wherein said first insulating film 15 is made of oxide film, and said second insulating film 16 is made of nitride film.

3) A semiconductor device manufacturing method, as cited in Claim 1, wherein said first insulating film 15 is made of nitride film, and said second insulating film 16 is made of oxide film.

4) A semiconductor device manufacturing method, as cited in one of the Claims 1, 2, and 3, wherein said first conduction-type refers to N-type impurities, and said second conduction-type refers to P-type impurities.

5) A semiconductor device manufacturing method, as cited in one of the Claims 1, 2, 3, and 4, wherein the process of forming said first sidewall space 15a is comprised of: a step of forming a photosensitive film on the second insulating film 16 after forming said first insulating film 15 and second insulating film 16; a step of anisotropic-etching said first insulating film 15 and second insulating film 16 using said photosensitive film as a mask after removing the photosensitive film in said first region.

6) A semiconductor device manufacturing method, as cited in one of the Claims 1, 2, 3, 4, and 5, wherein the process of forming said second

sidewall space 20 is comprised of: a step of forming a photosensitive film on said second insulation film 16 in said first and second regions; a step of forming the first insulating film sidewall space between the side surface of second gate electrode 13b and the second insulating film sidewall space, by forming the second insulating film sidewall space on the first insulating film 15 on the side surface of the second gate electrode 13b by anisotropic-etching the second insulating film 16 using the photosensitive film as a mask after removing the photosensitive film in said second region, and by anisotropic-etching said first insulating film 15 using the photosensitive film and second insulating film 16 as masks.

DETAILED DESCRIPTION OF THE INVENTION

(0001)

(Field of Industrial Application)

The present invention pertains to a method to manufacture a semiconductor device, particularly, to a technology for improving a short channel characteristic and for increasing a driving current of the device.

(0002)

(Prior Art)

With a pMOS device with a lightly doped drain (LDD) in general, diffusion of p^+ is greater than that of n^+. Therefore, the LDD region of p^- is

narrowed by p+ diffusion in the side surface, forming a deep junction and undercutting the short channel characteristic of a semiconductor device, which is a problem.

(0003)

There has been presented a thesis on a semiconductor device manufacturing method, whereby a short channel characteristic of the device is improved to increase the driving current (VLSI Symposium, 1991, pp. 85-86). More specifically, as shown in Fig. 3, a gate oxide film 2 is formed on a specific region on the semiconductor substrate 1, and after polysilicon is vapor-deposited on the gate oxide film 2, the patterns for gates, 3a, 3b, are formed on the nMOS region and pMOS region by photo-etching, respectively.

(0004)

Then, using the gates, 3a, 3b, of nMOS region and pMOS region as masks, ion implantation is applied to the semiconductor substrate 1 to form the n^- and p^- LDD regions, 4a, 4b, respectively. Then, after an insulating film is vapor-deposited on the semiconductor substrate, on which are formed the nMOS region and pMOS region, a sidewall space 5a is formed on the side surfaces of gates, 3a, 3b, of nMOS region and pMOS region by anisotropic etching, respectively.

(0005)

Then, after forming the n^+ region in the semiconductor substrate 1 by applying the ion implantation only to the nMOS region, the sidewall space 5a is formed on the side surface of sidewall space 5a of gate 3b of pMOS region by vapor-depositing an insulating film on the semiconductor substrate 1. As a result, the sidewall space (5a + 5b) of gate 3b in the pMOS region becomes much thicker than the sidewall space (5a) of gate 3a in the nMOS region. Subsequently, the p^+ region is formed on the semiconductor substrate 1 by applying the ion implantation only to the p^+ region.

(0006)

(Problems of the Prior Art to Be Addressed)

When this prior art semiconductor device manufacturing method is used for manufacturing a DRAM device having a cell transistor, as shown in Fig. 4, the adjacent sidewalls of the cell transistors are brought into contact due to the thick sidewall space, hindering the ion implantation for forming the n^+ region and the formation of contact holes for self-matching, which are the problems in manufacturing the next generation high-density DRAM device.

(0007)

The present invention, to solve the aforementioned problems, attempts to present a semiconductor device manufacturing method applicable to manufacturing a high-density DRAM device by improving a short channel characteristic and by increasing a driving current of the device.

(0008)

(Means to Solve the Problems)

The invention cited in Claim 1 claims a semiconductor device manufacturing method, whereby the following steps are successively performed:

a step of forming the gate insulating film on the semiconductor substrate having a first region and a second region;

a step of forming a first gate electrode and a second gate electrode on the first region and the second region on the semiconductor substrate, respectively;

a step of forming a first conduction-type low concentration impurity region in the first region near the edge of the first gate electrode base in the semiconductor substrate;

a step of forming a second conduction-type low concentration impurity region on the second region near the edge of the second gate electrode base on the semiconductor substrate;

a step of forming a first insulating film on the semiconductor substrate on which is formed the first and second electrodes;

a step of forming a second insulating film on the first insulating film;

a step of removing the second insulating film on the first region;

a step of forming a first sidewall space on the sidewall of the first gate electrode by anisotropic-etching the first insulating film on the first region;

a step of forming a first conduction-type high concentration impurity region near the edge of the base of the first gate electrode, on which the first sidewall space is formed, in the first region on the semiconductor substrate;

a step of forming a second sidewall space made of first insulating film and second insulating film on the side surface of the second gate electrode by anisotropic etching the first insulating film and second insulating film in the second region;

a step of forming a second conduction-type high concentration impurity region near the edge of the base of the second gate electrode on which is formed the second sidewall space in the second region on the semiconductor substrate.

(0009)

In the aforementioned structure, after the first insulating film and second insulating film are formed on the semiconductor substrate, on which are formed the first and second gate electrodes, the first sidewall space is formed by removing the second insulating film and anisotropic-etching the first insulating film in the first region. On the other hand, in the second region, the second sidewall space is formed by anisotropic-etching the first insulating film and second insulating film. More specifically, the first sidewall space is made of first insulating film, and the second sidewall space is made of first insulating film and second insulating film. Therefore, the second sidewall space becomes thicker than the first sidewall space, which improves the short channel characteristic of the semiconductor device.

(0010)

The invention of Claim 2 presents a structure, wherein the first insulating film is made of oxide film and the second insulating film is made of nitride film. In this structure, the first insulating film and second insulating film are made of oxide film and nitride film that have an excellent selectivity ratio in wet-etching, and therefore the sidewall space can be selectively formed in the first region or the second region.

(0011)

The invention of Claim 3 presents a structure, wherein the first insulating film is made of nitride film and the second insulating film is made of oxide film. In this structure, the first insulating film and the second insulating film are made of nitride film and oxide film that have an excellent selectivity ratio in wet etching, and therefore the sidewall space can be selectively formed in the first region or in the second region.

(0012)

The invention of Claim 4 claims the structure, wherein the first conduction-type refers to N-type impurities, and the second conduction-type refers to P-type impurities. In this structure, the first conductor contains the N-type impurities and the second conductor contains the P-type impurities, by which the channel characteristic is effectively improved.

(0013)

The invention of Claim 5 claims the process of forming the first sidewall space that is comprised of: a step of forming the photosensitive film on the second insulating film after forming the first insulating film and second insulating film; a step of anisotropic-etching the first insulating film and the second insulating film using the photosensitive film as a mask after removing the photosensitive film in the first region. In this process, the first

sidewall space is formed by anisotropic-etching the first insulating film and the second insulating film after removing the photosensitive film in the first region, and therefore the second region, in which is retained the photosensitive film, is not etched, making the etching step simpler.

(0014)

The invention of Claim 6 claims the process of forming the second sidewall space that is comprised of: a step of forming the photosensitive film on the second insulating film in the first region and in the second region; a step of forming the first insulating film sidewall space between the side surface of the second gate electrode and the second insulating film sidewall space, by forming the second insulating film sidewall space on the first insulating film on the second gate electrode side surface by anisotropic-etching the second insulating film using the photosensitive film as a mask after removing the photosensitive film in the second region, and by anisotropic-etching said first insulating film using said photosensitive film and second insulating film as masks.

(0015)

In this structure, the second sidewall space is formed by removing the photosensitive film in the second region, forming the second insulating sidewall space on the first insulating film by anisotropic-etching the second

insulating film, and by further forming the first insulating film sidewall space by anisotropic etching the first insulating film. Therefore, the first region, in which is retained the photosensitive film, is not etched, making the etching step simpler.

(0016)

(Embodiment)

The embodiment of the present invention is explained below. In the method to manufacture the semiconductor device of the present invention, as shown in Fig. 1(A), the gate insulating film 12 made of oxide film is formed on the semiconductor substrate 11 and, after polysilocon is vapor-deposited on the gate insulating film 12, photo-etching is applied to the nMOS region in the first region and to pMOS region in the second region on the semiconductor substrate to form the patterns for the polysilicon gates, 13a, 13b, respectively. Subsequently, after dividing the first region, a lightly doped drain (LDD) region 14 is formed as the first conduction-type n^- low concentration impurity region by ion implantation in the semiconductor substrate. After the second region is divided likewise, the LDD region 14b is formed as the second conduction-type p^- low concentration impurity region by ion implantation in the semiconductor substrate 11. Subsequently, on the semiconductor substrate 11, on which are

formed the first region and the second region, the first insulating film 15 made of oxide film is vapor-deposited by a chemical vapor deposition method, and the second insulating film 16 made of nitride film is vapor-deposited by a chemical vapor deposition method. In this case, the second insulating film can be formed by successively vapor-depositing the oxide film and the nitride film. Also, the first insulating film 15 may be made of nitride film and the second insulating film may be made of oxide film.

(0017)

Subsequently, as shown in Fig. 1(B), the photosensitive film (not shown in the figure) is coated on the second insulating film 16, and after exposing the first region by dividing and photo-etching the first region, the second insulating film 16 on the first region is removed by anisotropic etching using the photosensitive film as a mask. Subsequently, as shown in Fig. 1(C), the first conduction-type high concentration impurity region is formed on the semiconductor substrate 11 by anisotropic-etching the first insulating film on the first region using the photosensitive film (not shown in the figure) as a mask, forming the first sidewall space 15a on the side surface of the polysilicon gate 13a in the first region, and by performing the ion-implantation. Subsequently, the photosensitive film (not shown in the figure) is again coated on the first region and on the second region, and after

the second region is exposed, the first insulating film sidewall space is formed between the side surface of polysilicon gate 13 and the second insulating film sidewall space by forming the second insulating film sidewall space on the first insulating film 15 on the side surface of polysilicon gate 13 by applying the anisotropic etching using the photosensitive film as a mask and by anisotropic-etching the first insulating film 15 using the photosensitive film and second insulating film 16 as masks. As a result, the insulating film sidewall space 20 having a double-layer structure is formed. Subsequently, by ion implantation, the second conduction-type high concentration impurity region is formed on the semiconductor substrate 11. In this case, the sidewall space 20 can be also formed by successively vapor-depositing the oxide film, nitride film, and oxide film in this order.

(0018)

Accordingly, in the present invention, to selectively form the sidewall space in the pMOS region, the photo-etching is additionally applied after the CVD nitride film is vapor-deposited, or the CVD nitride film and oxide film are successively vapor-deposited. As a result, merely by adding the nitride film (Si_3N_4) vapor-deposition step, various problems that will arise when the prior art semiconductor device manufacturing method is applied to

the next generation high density DRAM can be solved. In addition, to improve the characteristics of pMOS device, the thickness of the sidewall space of pMOS device can be made thicker by about 500 – 1,000 Å than the sidewall space thickness of nMOS device.

(0019)

Fig. 2 shows the structure of a cell transistor when the semiconductor device manufacturing method of the present invention is used for manufacturing a DRAM device. As shown in the figure, since the sidewall space 15a and sidewall space 20 are separately formed in the adjacent transistor regions, the ion implantation and self-matching contact formation are possible, which contributes to the manufacturing of the next generation 256 MB DRAM device.

(0020)

In addition, since the thick space is selectively formed only in the pMOS region by dry-etching after forming the double-layer space using the oxide film and nitride film layers that have an excellent selectivity ratio in wet-etching, retaining it only in the pMOS region, and by removing the nitride film in the nMOS region, the cell transistors do not contact with each other and the ion implantation can be performed even if this method is used for manufacturing the prior art DRAM device.

(0021)

(Advantage)

As explained above, by the invention claimed in Claim 1, the short channel characteristic of a semiconductor device can be improved and the driving current of the device can be increased. Therefore, the method of the present invention can be applied for manufacturing the next generation high density DRAM. By the invention claimed in Claim 2 or Claim 3, the sidewall space in the first region or in the second region can be selectively formed.

(0022)

By the invention claimed in Claim 4, the channel characteristic of a semiconductor device can be improved. By the inventions claimed in Claim 5 or Claim 6, the etching steps can be simplified.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 shows the manufacturing method of the semiconductor device of the present invention; (A) illustrates the steps of forming the first insulating film and second insulating film; (B) illustrates the steps of removing the second insulating film in the first region; (C) illustrates the steps of completing the sidewall space.

Fig. 2 illustrates the semiconductor device manufacturing method of the present invention being applied to a DRAM manufacturing method.

Fig. 3 illustrates the steps of the prior art semiconductor manufacturing method.

Fig. 4 illustrates the prior art semiconductor manufacturing method being applied to a DRAM device manufacturing method.

11. semiconductor substrate

12. gate insulating film

13a, 13b. polysilicon gate

14a, 14b. low concentration impurity region

15. first insulating film

15a. first sidewall space

16. second insulating film

20. second sidewall space